

# DATA SHEET

## **74ALVCH32501**

**36-bit universal bus transceiver with  
direction pin; 3-state**

Product specification  
Supersedes data of 2000 Mar 16

2004 Oct 13

## 36-bit universal bus transceiver with direction pin; 3-state

### 74ALVCH32501

#### FEATURES

- 3-state non-inverting outputs for bus oriented applications
- Wide supply voltage range of 1.2 V to 3.6 V
- Complies with JEDEC standard no. 8-1A
- Current drive  $\pm 24$  mA at 3.0 V
- Universal bus transceiver with D-type latches and D-type flip-flops capable of operating in transparent, latched or clocked mode
- CMOS low power consumption
- Direct interface with TTL levels
- All inputs have bus-hold circuitry
- Output drive capability 50  $\Omega$  transmission lines at 85 °C
- Plastic fine-pitch ball grid array package.

#### DESCRIPTION

The 74ALVCH32501 is a high-performance CMOS product designed for  $V_{CC}$  operation at 2.5 V and 3.3 V.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The 74ALVCH32501 can be used as two 18-bit transceivers or one 36-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. Data flow in each direction is controlled by output enable ( $OE_{AB}$  and  $\overline{OE}_{BA}$ ), latch enable ( $LE_{AB}$  and  $LE_{BA}$ ), and clock inputs ( $CP_{AB}$  and  $CP_{BA}$ ). For A-to-B data flow, the device operates in the transparent mode when  $LE_{AB}$  is HIGH. When input  $LE_{AB}$  is LOW, the A data is latched if input  $CP_{AB}$  is held at a HIGH or LOW level. If input  $LE_{AB}$  is LOW, the A data is stored in the latch/flip-flop on the LOW-to-HIGH transition of  $CP_{AB}$ . When input  $OE_{AB}$  is HIGH, the outputs are active. When input  $OE_{AB}$  is LOW, the outputs are in the high-impedance state.

Data flow for B-to-A is similar to that of A-to-B, but uses inputs  $\overline{OE}_{BA}$ ,  $LE_{BA}$  and  $CP_{BA}$ . The output enables are complementary ( $OE_{AB}$  is active HIGH, and  $\overline{OE}_{BA}$  is active LOW).

To ensure the high-impedance state during power-up or power-down, pin  $\overline{OE}_{BA}$  should be tied to  $V_{CC}$  through a pull-up resistor and pin  $OE_{AB}$  should be tied to GND through a pull-down resistor. The minimum value of the resistor is determined by the current-sinking or current-sourcing capability of the driver.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25$  °C;  $t_r = t_f \leq 2.5$  ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 30$ pF; $V_{CC} = 2.5$ V	2.8	ns
		$C_L = 50$ pF; $V_{CC} = 3.3$ V	3.0	ns
$C_I$	input capacitance		4.0	pF
$C_{I/O}$	input/output capacitance		8.0	pF
$C_{PD}$	power dissipation capacitance per latch	$V_I = GND$ to $V_{CC}$ ; note 1		
		outputs enabled	21	pF
	outputs disabled	3	pF	

#### Note

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz;

$f_o$  = output frequency in MHz;

$C_L$  = output load capacitance in pF;

$V_{CC}$  = supply voltage in Volts;

$N$  = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

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**FUNCTION TABLE**

See notes 1 and 2.

INPUT				INTERNAL REGISTERS	OUTPUT	OPERATING MODE
nOE <sub>AB</sub>	nLE <sub>AB</sub>	nCP <sub>AB</sub>	nA <sub>n</sub>		nB <sub>n</sub>	
L	H	X	X	X	Z	disabled
L	↓	X	h	H	Z	disabled; latch data
L	↓	X	l	L	Z	
L	L	H or L	X	NC	Z	disabled; hold data
L	L	↑	h	H	Z	disabled; clock data
L	L	↑	l	L	Z	
H	H	X	H	H	H	transparent
H	H	X	L	L	L	
H	↓	X	h	H	H	latch data and display
H	↓	X	l	L	L	
H	L	↑	h	H	H	clock data and display
H	L	↑	l	L	L	
H	L	H or L	X	H	H	hold data and display
H	L	H or L	X	L	L	

**Notes**

1. A-to-B data flow is shown; B-to-A flow is similar but uses  $\overline{\text{nOE}}_{\text{BA}}$ ,  $\text{nLE}_{\text{BA}}$  and  $\text{nCP}_{\text{BA}}$ .
2. H = HIGH voltage level;  
h = HIGH voltage level on set-up time prior to the enable or clock transition;  
L = LOW voltage level;  
l = LOW voltage level on set-up time prior to the enable or clock transition;  
NC = no change;  
X = don't care;  
↑ = LOW-to-HIGH enable or clock transition;  
↓ = HIGH-to-LOW enable or clock transition;  
Z = high impedance OFF-state.

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE				
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE
74ALVCH32501EC	-40 °C to +85 °C	114	LFBGA114	plastic	SOT537-1

PINNING

SYMBOL	DESCRIPTION
nA <sub>n</sub>	data inputs
nB <sub>n</sub>	data outputs
GND	ground (0 V)
V <sub>CC</sub>	DC supply voltage
nOE <sub>AB</sub>	output enable inputs A to B (active HIGH)
n $\overline{O}E_{BA}$	output enable inputs B to A (active LOW)
nLE <sub>AB</sub>	latch enable inputs A to B
nLE <sub>BA</sub>	latch enable inputs B to A
nCP <sub>AB</sub>	clock input A to B
nCP <sub>BA</sub>	clock input B to A

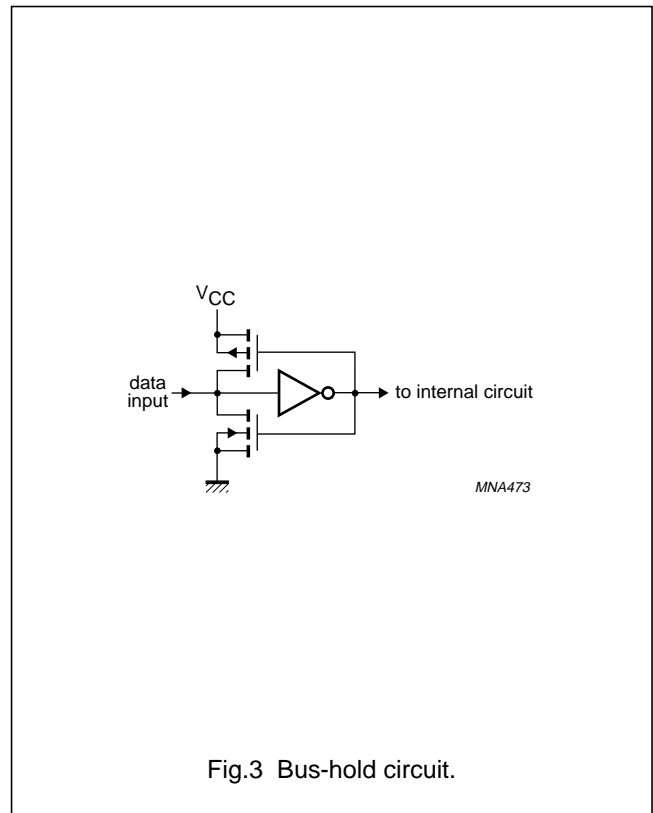
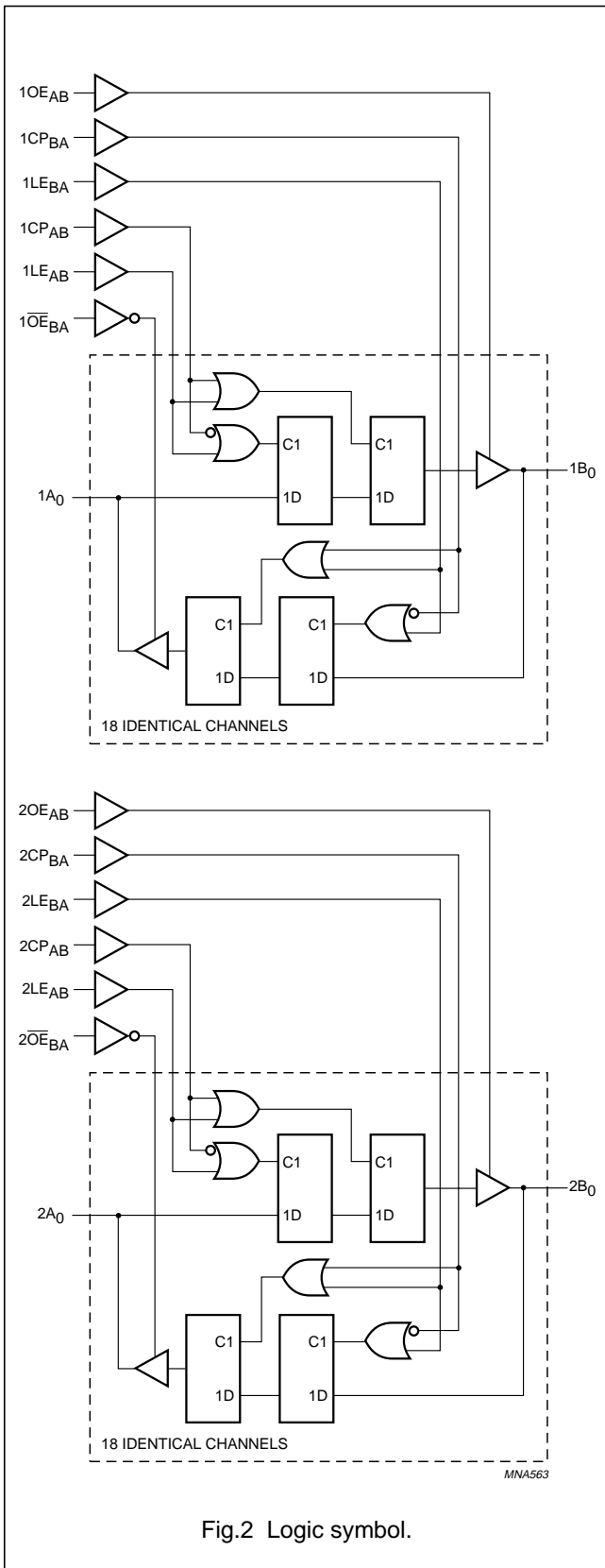
6	1B <sub>1</sub>	1B <sub>3</sub>	1B <sub>5</sub>	1B <sub>7</sub>	1B <sub>9</sub>	1B <sub>11</sub>	1B <sub>13</sub>	1B <sub>14</sub>	1B <sub>16</sub>	n.c.	2B <sub>1</sub>	2B <sub>3</sub>	2B <sub>5</sub>	2B <sub>7</sub>	2B <sub>9</sub>	2B <sub>11</sub>	2B <sub>13</sub>	2B <sub>14</sub>	2B <sub>16</sub>
5	1B <sub>0</sub>	1B <sub>2</sub>	1B <sub>4</sub>	1B <sub>6</sub>	1B <sub>8</sub>	1B <sub>10</sub>	1B <sub>12</sub>	1B <sub>15</sub>	1B <sub>17</sub>	2CP <sub>AB</sub>	2B <sub>0</sub>	2B <sub>2</sub>	2B <sub>4</sub>	2B <sub>6</sub>	2B <sub>8</sub>	2B <sub>10</sub>	2B <sub>12</sub>	2B <sub>15</sub>	2B <sub>17</sub>
4	1CP <sub>AB</sub>	GND	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1CP <sub>BA</sub>	GND	GND	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2CP <sub>BA</sub>	GND
3	1LE <sub>AB</sub>	1OE <sub>AB</sub>	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	1 $\overline{O}E_{BA}$	1LE <sub>BA</sub>	2OE <sub>AB</sub>	GND	V <sub>CC</sub>	GND	GND	V <sub>CC</sub>	GND	2 $\overline{O}E_{BA}$	2LE <sub>BA</sub>
2	1A <sub>0</sub>	1A <sub>2</sub>	1A <sub>4</sub>	1A <sub>6</sub>	1A <sub>8</sub>	1A <sub>10</sub>	1A <sub>12</sub>	1A <sub>15</sub>	1A <sub>17</sub>	2LE <sub>AB</sub>	2A <sub>0</sub>	2A <sub>2</sub>	2A <sub>4</sub>	2A <sub>6</sub>	2A <sub>8</sub>	2A <sub>10</sub>	2A <sub>12</sub>	2A <sub>15</sub>	2A <sub>17</sub>
1	1A <sub>1</sub>	1A <sub>3</sub>	1A <sub>5</sub>	1A <sub>7</sub>	1A <sub>9</sub>	1A <sub>11</sub>	1A <sub>13</sub>	1A <sub>14</sub>	1A <sub>16</sub>	n.c.	2A <sub>1</sub>	2A <sub>3</sub>	2A <sub>5</sub>	2A <sub>7</sub>	2A <sub>9</sub>	2A <sub>11</sub>	2A <sub>13</sub>	2A <sub>14</sub>	2A <sub>16</sub>
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W

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Fig.1 Pin configuration.

36-bit universal bus transceiver with direction pin;  
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### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage	2.5 V range (for maximum speed performance at 30 pF output load)	2.3	2.7	V
		3.3 V range (for maximum speed performance at 50 pF output load)	3.0	3.6	V
V <sub>I</sub>	input voltage		0	V <sub>CC</sub>	V
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	input rise and fall time ratios (Δt/ΔV)	V <sub>CC</sub> = 1.2 V to 2.7 V	0	20	ns/V
		V <sub>CC</sub> = 2.7 V to 3.6 V	0	10	ns/V

### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
V <sub>I</sub>	input voltage	for control pins; note 1	-0.5	+4.6	V
		for data input pins; note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	input diode current	V <sub>I</sub> < 0 V	-	-50	mA
I <sub>OK</sub>	output clamping diode current	V <sub>O</sub> < 0 V; note 1	-	50	mA
V <sub>O</sub>	output voltage	see note 1	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>O</sub>	output sink current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	-50	mA
I <sub>CC</sub> , I <sub>GND</sub>	V <sub>CC</sub> or GND current		-	±100	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	power dissipation	T <sub>amb</sub> = -40 °C to +85 °C; note 2	-	1000	mW

### Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. Above 55 °C the value of P<sub>tot</sub> derates linearly with 1.8 mW/K.

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## DC CHARACTERISTICS

Over recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP. <sup>(1)</sup>	MAX.	UNIT
		OTHER	V <sub>CC</sub> (V)				
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>							
V <sub>IH</sub>	HIGH-level input voltage		2.3 to 2.7	1.7	1.2	–	V
			2.7 to 3.6	2.0	1.5	–	V
V <sub>IL</sub>	LOW-level input voltage		2.3 to 2.7	–	1.2	0.7	V
			2.7 to 3.6	–	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -100 μA	2.3 to 3.6	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	–	V
		I <sub>O</sub> = -6 mA	2.3	V <sub>CC</sub> - 0.3	V <sub>CC</sub> - 0.08	–	V
		I <sub>O</sub> = -12 mA	2.3	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.26	–	V
		I <sub>O</sub> = -12 mA	2.7	V <sub>CC</sub> - 0.5	V <sub>CC</sub> - 0.14	–	V
		I <sub>O</sub> = -12 mA	3.0	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.09	–	V
		I <sub>O</sub> = -24 mA	3.0	V <sub>CC</sub> - 1.0	V <sub>CC</sub> - 0.28	–	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 100 μA	2.3 to 3.6	–	GND	0.20	V
		I <sub>O</sub> = 6 mA	2.3	–	0.07	0.40	V
		I <sub>O</sub> = 12 mA	2.3	–	0.15	0.70	V
		I <sub>O</sub> = 12 mA	2.7	–	0.14	0.40	V
		I <sub>O</sub> = 24 mA	3.0	–	0.27	0.55	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	2.3 to 3.6	–	±0.1	±5	μA
I <sub>OZ</sub>	3-state output OFF-state current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND; note 2	2.3 to 3.6	–	0.1	±10	μA
I <sub>CC</sub>	quiescent supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A	2.3 to 3.6	–	0.4	80	μA
ΔI <sub>CC</sub>	additional quiescent supply current given per data I/O pin with bus-hold	V <sub>I</sub> = V <sub>CC</sub> - 0.6 V; I <sub>O</sub> = 0 A	2.7 to 3.6	–	150	750	μA
I <sub>BHL</sub>	bus-hold LOW sustaining current	V <sub>I</sub> = 0.7 V; note 3	2.3	45	–	–	μA
		V <sub>I</sub> = 0.8 V; note 3	3.0	75	150	–	μA
I <sub>BHH</sub>	bus-hold HIGH sustaining current	V <sub>I</sub> = 1.7 V; note 3	2.3	-45	–	–	μA
		V <sub>I</sub> = 2.0 V; note 3	3.0	-75	-175	–	μA
I <sub>BHLO</sub>	bus-hold LOW overdrive current	note 3	3.6	500	–	–	μA
I <sub>BHHO</sub>	bus-hold HIGH overdrive current	note 3	3.6	-500	–	–	μA

### Notes

1. All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.
2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.
3. Valid for data inputs of bus-hold parts.

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**AC CHARACTERISTICS** $T_{amb} = -40\text{ °C to }+85\text{ °C}; GND = 0\text{ V}$ 

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	$C_L$				
<b><math>V_{CC} = 2.3\text{ V to }2.7\text{ V}; t_r = t_f \leq 2.0\text{ ns}; \text{ note 1}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay $nA_n$ to $nB_n$ ; $nB_n$ to $nA_n$	see Figs 4 and 8	30 pF	1.0	2.8	5.1	ns
	$nLE_{BA}$ to $nA_n$ ; $nLE_{AB}$ to $nB_n$	see Figs 5 and 8	30 pF	1.1	3.5	6.1	ns
	$nCP_{BA}$ to $nA_n$ ; $nCP_{AB}$ to $nB_n$	see Figs 5 and 8	30 pF	1.0	3.3	6.1	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8	30 pF	1.0	2.5	5.8	ns
	3-state output enable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8	30 pF	1.3	2.8	6.3	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8	30 pF	1.5	2.5	6.2	ns
	3-state output disable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8	30 pF	1.3	2.5	5.3	ns
$t_W$	$nLE_{AB}$ or $nLE_{BA}$ pulse width HIGH	see Figs 5 and 8	30 pF	3.3	0.8	–	ns
	$nCP_{AB}$ or $nCP_{BA}$ pulse width HIGH or LOW	see Figs 5 and 8	30 pF	3.3	2.0	–	ns
$t_{su}$	set-up time $nA_n$ before $nCP_{AB}\uparrow$ or $nB_n$ before $nCP_{BA}\uparrow$	see Figs 7 and 8	30 pF	1.7	0.1	–	ns
	set-up time CP HIGH or LOW $nA_n$ before $nLE_{AB}\downarrow$ or $nB_n$ before $nLE_{BA}\downarrow$	see Figs 7 and 8	30 pF	1.1	0.1	–	ns
$t_h$	hold time $nA_n$ after $nCP_{AB}\uparrow$ or $nB_n$ after $nCP_{BA}\uparrow$	see Figs 7 and 8	30 pF	1.7	0.3	–	ns
	hold time CP HIGH or LOW $nA_n$ after $nLE_{AB}\downarrow$ or $nB_n$ after $nLE_{BA}\downarrow$	see Figs 7 and 8	30 pF	1.6	0.3	–	ns
$f_{max}$	maximum clock frequency	see Figs 5 and 8	30 pF	150	330	–	MHz
<b><math>V_{CC} = 2.7\text{ V}; t_r = t_f \leq 2.5\text{ ns}; \text{ note 2}</math></b>							
$t_{PHL}/t_{PLH}$	propagation delay $nA_n$ to $nB_n$ ; $nB_n$ to $nA_n$	see Figs 4 and 8	50 pF	–	3.0	4.6	ns
	$nLE_{BA}$ to $nA_n$ ; $nLE_{AB}$ to $nB_n$	see Figs 5 and 8	50 pF	–	3.6	5.3	ns
	$nCP_{BA}$ to $nA_n$ ; $nCP_{AB}$ to $nB_n$	see Figs 5 and 8	50 pF	–	3.4	5.6	ns
$t_{PZH}/t_{PZL}$	3-state output enable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8	50 pF	–	2.7	5.3	ns
	3-state output enable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8	50 pF	–	3.3	6.0	ns
$t_{PHZ}/t_{PLZ}$	3-state output disable time $nOE_{AB}$ to $nB_n$	see Figs 6 and 8	50 pF	–	3.6	5.7	ns
	3-state output disable time $n\overline{OE}_{BA}$ to $nA_n$	see Figs 6 and 8	50 pF	–	3.3	4.6	ns
$t_W$	pulse width $nLE_{AB}$ or $nLE_{BA}$ HIGH	see Figs 5 and 8	50 pF	3.3	0.7	–	ns
	pulse width $nCP_{AB}$ or $nCP_{BA}$ HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.4	–	ns
$t_{su}$	set-up time $nA_n$ before $nCP_{AB}\uparrow$ or $nB_n$ before $nCP_{BA}\uparrow$	see Figs 7 and 8	50 pF	+1.4	–0.1	–	ns
	set-up time CP HIGH or LOW $nA_n$ before $nLE_{AB}\downarrow$ or $nB_n$ before $nLE_{BA}\downarrow$	see Figs 7 and 8	50 pF	+1.0	–0.2	–	ns



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SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	C <sub>L</sub>				
t <sub>h</sub>	hold time nA <sub>n</sub> after nCP <sub>AB</sub> ↑ or nB <sub>n</sub> after nCP <sub>BA</sub> ↑	see Figs 7 and 8	50 pF	1.6	0.3	–	ns
	hold time CP HIGH or LOW nA <sub>n</sub> after nLE <sub>AB</sub> ↓ or nB <sub>n</sub> after nLE <sub>BA</sub> ↓	see Figs 7 and 8	50 pF	1.5	0.1	–	ns
f <sub>max</sub>	maximum clock frequency	see Figs 5 and 8	50 pF	150	333	–	MHz
<b>V<sub>CC</sub> = 3.0 V to 3.6 V; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns; note 3</b>							
t <sub>PHL</sub> /t <sub>PLH</sub>	propagation delay nA <sub>n</sub> to nB <sub>n</sub> ; nB <sub>n</sub> to nA <sub>n</sub>	see Figs 4 and 8	50 pF	1.0	3.0	4.2	ns
	nLE <sub>BA</sub> to nA <sub>n</sub> ; nLE <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8	50 pF	1.3	3.4	4.8	ns
	nCP <sub>BA</sub> to nA <sub>n</sub> ; nCP <sub>AB</sub> to nB <sub>n</sub>	see Figs 5 and 8	50 pF	1.4	3.3	4.9	ns
t <sub>PZH</sub> /t <sub>PZL</sub>	3-state output enable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8	50 pF	1.0	2.4	4.6	ns
	3-state output enable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8	50 pF	1.1	2.5	5.0	ns
t <sub>PHZ</sub> /t <sub>PLZ</sub>	3-state output disable time nOE <sub>AB</sub> to nB <sub>n</sub>	see Figs 6 and 8	50 pF	1.4	2.9	5.0	ns
	3-state output disable time nOE <sub>BA</sub> to nA <sub>n</sub>	see Figs 6 and 8	50 pF	1.3	3.1	4.2	ns
t <sub>w</sub>	pulse width nLE <sub>AB</sub> or nLE <sub>BA</sub> HIGH	see Figs 5 and 8	50 pF	3.3	0.9	–	ns
	pulse width nCP <sub>AB</sub> or nCP <sub>BA</sub> HIGH or LOW	see Figs 5 and 8	50 pF	3.3	1.1	–	ns
t <sub>su</sub>	set-up time nA <sub>n</sub> before nCP <sub>AB</sub> ↑ or nB <sub>n</sub> before nCP <sub>BA</sub> ↑	see Figs 7 and 8	50 pF	+1.3	–0.3	–	ns
	set-up time CP HIGH or LOW nA <sub>n</sub> before nLE <sub>AB</sub> ↓ or nB <sub>n</sub> before nLE <sub>BA</sub> ↓	see Figs 7 and 8	50 pF	1.0	0.3	–	ns
t <sub>h</sub>	hold time nA <sub>n</sub> after nCP <sub>AB</sub> ↑ or nB <sub>n</sub> after nCP <sub>BA</sub> ↑	see Figs 7 and 8	50 pF	+1.3	–0.4	–	ns
	hold time CP HIGH or LOW nA <sub>n</sub> after nLE <sub>AB</sub> ↓ or nB <sub>n</sub> after nLE <sub>BA</sub> ↓	see Figs 7 and 8	50 pF	1.2	0.1	–	ns
f <sub>max</sub>	maximum clock frequency	see Figs 5 and 8	50 pF	150	340	–	MHz

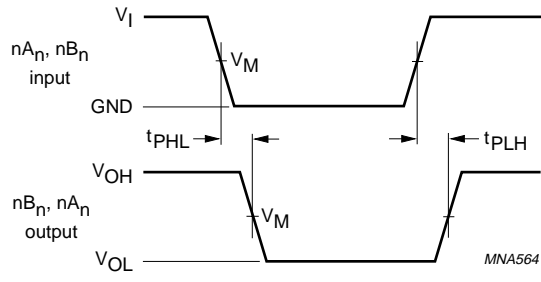
**Notes**

1. All typical values are measured at V<sub>CC</sub> = 2.5 V and T<sub>amb</sub> = 25 °C.
2. All typical values are measured at T<sub>amb</sub> = 25 °C.
3. All typical values are measured at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25 °C.

36-bit universal bus transceiver with direction pin;  
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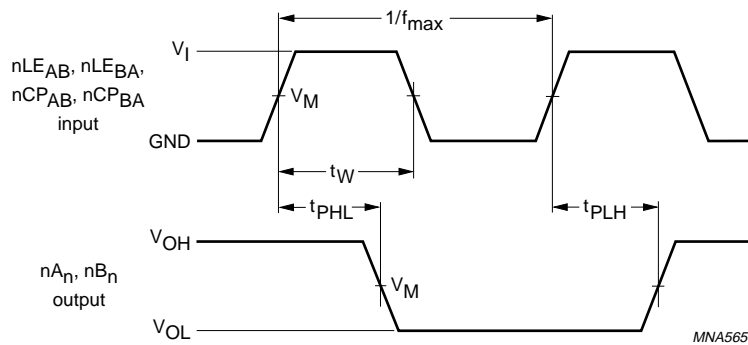
AC WAVEFORMS



V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.4 Input nA<sub>n</sub>, nB<sub>n</sub> to output nB<sub>n</sub>, nA<sub>n</sub> propagation delay times.



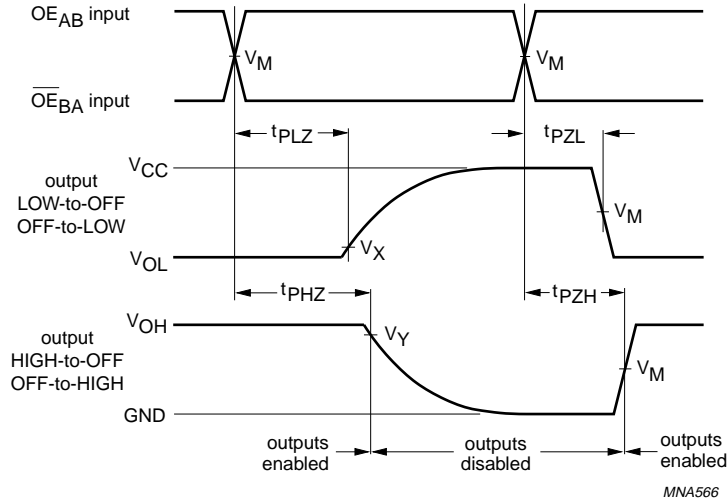
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.5 Latch enable input (nLE<sub>AB</sub>, nLE<sub>BA</sub>) and clock input (nCP<sub>AB</sub>, nCP<sub>BA</sub>) to output propagation delays and their pulse width.

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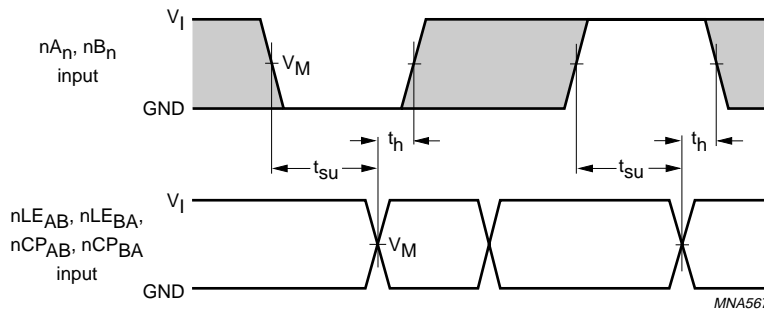
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V <sub>CC</sub>	V <sub>M</sub>	V <sub>X</sub>	V <sub>Y</sub>	V <sub>I</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>OL</sub> + 150 mV	V <sub>OH</sub> - 150 mV	V <sub>CC</sub>
2.7 V	1.5 V	V <sub>OL</sub> + 300 mV	V <sub>OH</sub> - 300 mV	2.7 V
3.0 V to 3.6 V	1.5 V	V <sub>OL</sub> + 300 mV	V <sub>OH</sub> - 300 mV	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.6 3-state enable and disable times.



The shaded areas indicate when the input is permitted to change for predictable output performance.

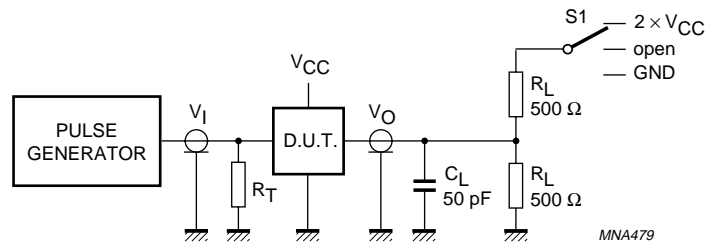
V <sub>CC</sub>	V <sub>M</sub>	V <sub>I</sub>
2.3 V to 2.7 V	0.5 × V <sub>CC</sub>	V <sub>CC</sub>
2.7 V	1.5 V	2.7 V
3.0 V to 3.6 V	1.5 V	2.7 V

V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage drop that occur with the output load.

Fig.7 Data set-up and hold times for the nA<sub>n</sub> and nB<sub>n</sub> inputs to the nLE<sub>AB</sub>, nLE<sub>BA</sub>, nCP<sub>AB</sub> and nCP<sub>BA</sub> inputs.

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TEST	S1
$t_{PLH}/t_{PHL}$	open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

Definitions for test circuit:

$R_L$  = Load resistor.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to the output impedance  $Z_0$  of the pulse generator.

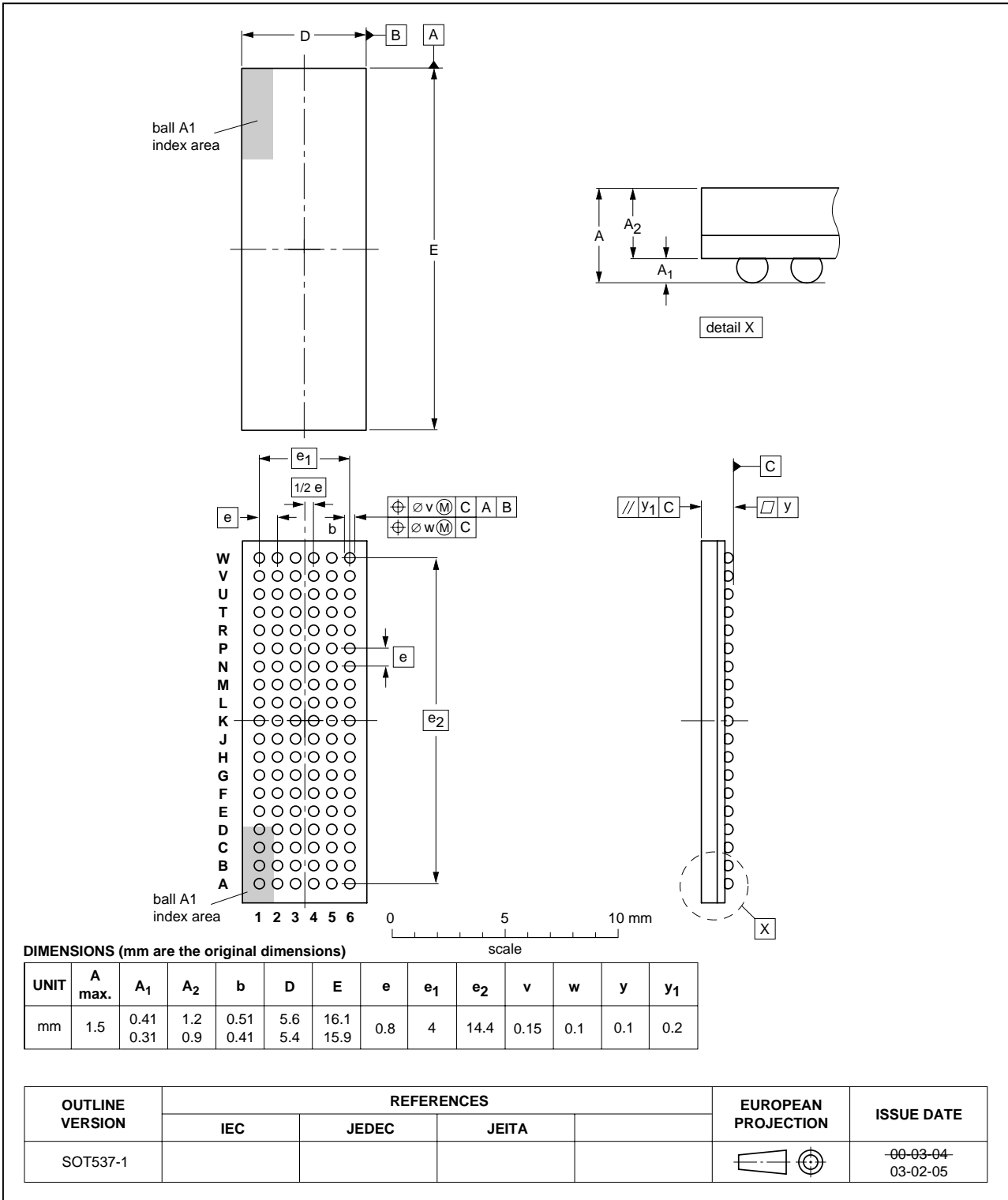
Fig.8 Load circuitry for switching times.

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PACKAGE OUTLINE

LFBGA114: plastic low profile fine-pitch ball grid array package; 114 balls; body 16 x 5.5 x 1.05 mm SOT537-1



# 36-bit universal bus transceiver with direction pin; 3-state

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## DATA SHEET STATUS

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I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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